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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/977,251	10/16/2001	Myung Sub Sim	K-0317	2253

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EXAMINER	
HO, THOMAS M	
ART UNIT	**PAPER NUMBER**
2134	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/977,251	SIM, MYUNG SUB	
	Examiner	Art Unit	
	Thomas M. Ho	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending.

Claim Objections

The Examiner should like it clarified to the record, whether the equation in claim 6, line four should recite "$E_i(k) =$" or "$E_1(k) =$". For purposes of examination, the Examiner has read this as the letter "i" though it resembles the number 1 as this equation appears to dictate the interleaving mechanism.

Claim Rejections - 35 USC § 112

2. Claim 6 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the function a(k).

Applicant has not defined this function in the claim. Such a function must be newly defined in the claim to give meaning to the expression in the context of the claim. Applicant states in page 8 of the specification that a(k) is an interleaving function defined by the interleaver of the turbo decoder. Such a stipulation in the claim would be sufficient to have this rejection under 35 USC 112 withdrawn.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Stralen et al., US patent 6304996.

In reference to claim 1:

Van Stralen et al. (Figure 1) discloses a method for performing turbo decoding, comprising:

- Primarily decoding signals received from a transmission system and storing the primarily decoded signals in a specific area of a memory, where the primary decoding signals are the signals of the top code parity data, the systematic data, and the bottom code parity data, and where the decoded signal is stored in the probability estimate memory.
- Interleaving the primarily decoded signals stored in the memory to change their order and secondarily decoding the interleaved signals, where the top and bottom signals are interleaved (Column 3, line 64- Column 4, line 4) et seq. and then run through the map decoder. (Figure 1, Item 14)

- Deinterleaving the secondarily decoded signals and storing the deinterleaved signals in the specific address space. (Figure 1, Items 22, 24)

In reference to claim 2:

Van Stralen et al. discloses the method of claim 1, wherein the primary decoding and the secondary decoding are iterated n times using a Maximum A posteriori (MAP) algorithm, where the decoder is a MAP decoder. (Figure 1, Items 12, 14) & (Column 1, lines 45-50)

In reference to claim 3:

Van Stralen et al. discloses the method of claim 2, wherein the primary decoding is performed using a current transmission system signal of the transmission system signals and an (n-1)^n iteration signal of the secondarily decoded signals,where both the alpha and beta functions(understood in the art to as the forward and backward state probability functions) are recursively defined (Column 3, lines 10-45) , making their computations (n-1)n iteration signals of the secondarily decoded values.

In reference to claim 4:

Van Stralen et al. discloses the method of claim 1, wherein the secondary decoding is performed using the transmission system signals and the primarily decoded signals, where the secondary decoding is the Map decoder (Figure 1, Item 14) and is performed using the original top code and bottom code signals.

In reference to claim 5:

Van Stralen et al. discloses the method of claim 1, wherein the interleaving operation, the secondarily decoding , and the deinterleaving operation are implemented simulataneously, where all the operations are implemented at the same time. (Figure 1)

In reference to claim 6:

Van Stralen et al. discloses a method for performing turbo decoding, comprising:

- Primarily decoding signals received from a transmission system and storing the primarily decoded signals into a specific address space of a memory. (Figure 1, Item 24)
- Interleaving the primarily decoded signals stored in the memory by an equation $E_i(k) = E(a(k))$, wherein k= 1,2,...,s, s is a code block size, and E(k) is a MAP decoded signal; (Figure 1, "interleavers") (Column 3, lines 64- Column 4, line 4) et seq.
- Secondarily decoding the interleaved signals in turn; (Figure 1, Item 14)
- Deinterleaving the secondarily decoded signals by an equation $E_d(a(k)) = E(k)$ wherein k = 1,2,...,s, s is the code block size and the E(k) is the MAP decoded signal; (Figure 1, Item 22) & (Column 3, lines 64- Column 4, line 4) et seq.
- Storing the deinterleaved signals in a predetermined region of the memory indicated by a(k). (Figure 1, Item 24) & (Column 3, lines 64- Column 4, line 4) et seq.

In reference to claim 11:

Van Stralen et al. discloses a method for performing turbo decoding, comprising:

- Primarily decoding composite signals comprising systematic symbols x_k,$(n-1)^{th}$ iteration extrinsic information, and parity symbols y_k; (Column 3, lines 10-45)
- Storing the primarily decoded composite signals in a specific address space of a memory; (Figure 1, Item 24)
- Interleaving the signals stored in the memory and secondarily decoding a second composite of the parity symbols y_k and the interleaved signals to generate n^{th} iteration extrinsic information. (Figure 1, "interleavers") (Column 3, lines 64- Column 4, line 4) et seq. & (Column 3, lines 10-45)
- Deinterleaving the secondarily decoded signals and storing the deinterleaved signals in the specific address space. (Figure 1, Items 22, 24)

Claims 7-10 are rejected for the same reasons as claims 2-5, respectively.

Claims 12-15 are rejected for the same reasons as claims 2-5, respectively.

5. Claims 1-15 are further rejected under 35 U.S.C. 102(e) as being anticipated by the prior art as disclosed by the Applicant. Applicant describes in detail the background of the related art to which Applicant's invention is improving upon in Figures 1 and 2. Applicant discloses the nature of these figures in the specification on pages 1-4. Through this disclosure of the prior art is made by the applicant, the applicant's claims are broad enough that they read upon it.

In reference to claim 1:

(Figures 1 & 2) discloses a method for performing turbo decoding, comprising:

- Primarily decoding signals received from a transmission system and storing the primarily decoded signals in a specific area of a memory, where the primary signals are decoded using MAP decoder D1 and stored in memory 106. (Figure 1)
- Interleaving the primarily decoded signals stored in the memory to change their order and secondarily decoding the interleaved signals, where the primarily decoded signals from the memory are interleaved by interleaver 102. (Figure 1)
- Deinterleaving the secondarily decoded signals and storing the deinterleaved signals in the specific address space, where the secondarily decoded signals are decoded by MAP decoder D2 and deinterleaved (Figure 1) and stored in a specific address space. (Figure 2)

In reference to claim 2:

Figures 1 & 2 discloses the method of claim 1, wherein the primary decoding and the secondary decoding are iterated n times using a Maximum A posteriori (MAP) algorithm, where the decoder used is MAP decoder which implements the MAP algorithm.

In reference to claim 3:

Figures 1 & 2 discloses the method of claim 2, wherein the primary decoding is performed using a current transmission system signal of the transmission system signals and an $(n-1)^n$ iteration signal of the secondarily decoded signals, where the primary decoding input is performed using the transmission signal x_k and the $(N-1)^{th}$ external data (dk).

In reference to claim 4:

Figures 1 & 2 discloses the method of claim 1, wherein the secondary decoding is performed using the transmission system signals and the primarily decoded signals, where the primarily decoded signals are sent from the interleaver as input to the secondary decoder, as is the transmission system signal y_k (parity)

In reference to claim 5:

Figures 1 & 2 discloses the method of claim 1, wherein the interleaving operation, the secondarily decoding, and the deinterleaving operation are implemented simulataneously, where the system works on all three functions simultaneously.

In reference to claim 6:

(Figures 1 & 2) discloses a method for performing turbo decoding, comprising:

- Primarily decoding signals received from a transmission system and storing the primarily decoded signals into a specific address space of a memory. (Item 101)
- Interleaving the primarily decoded signals stored in the memory by an equation $E_i(k) = E(a(k))$, wherein $k= 1,2,\ldots,s$, s is a code block size, and E(k) is a MAP decoded signal; (Item 102)
- Secondarily decoding the interleaved signals in turn; (Item 103)

- Deinterleaving the secondarily decoded signals by an equation $E_d(a(k)) = E(k)$ wherein k = 1,2,...,s, s is the code block size and the E(k) is the MAP decoded signal; (Items 104, 105) & (Figure 2)
- Storing the deinterleaved signals in a predetermined region of the memory indicated by a(k). (Item 106)

In reference to claim 11:

(Figures 1 & 2) discloses a method for performing turbo decoding, comprising:

- Primarily decoding composite signals comprising systematic symbols x_k,$(n-1)^{th}$ iteration extrinsic information, and parity symbols y_k, where these signals are input into MAP decoder 101.
- Storing the primarily decoded composite signals in a specific address space of a memory. (Item 106)
- Interleaving the signals stored in the memory and secondarily decoding a second composite of the parity symbols y_k and the interleaved signals to generate n^{th} iteration extrinsic information. (Item 102)
- Deinterleaving the secondarily decoded signals and storing the deinterleaved signals in the specific address space. (Items 104, 105) & (Figure 2)

Claims 7-10 are rejected for the same reasons as claims 2-5, respectively.

Claims 12-15 are rejected for the same reasons as claims 2-5, respectively.

Conclusion

6. The following art not relied upon is made of record:

- US patent 6192501 discloses a MAP decoder for trellis code words.
- "Near Shannon Limit Error – Correcting Coding and Decoding: Turbo Codes", IEEE 1993, Berrou et al. discloses what a turbo code is and the theory behind it.
- US patent 6392572 discloses a buffer architecture for a turbo decoder.
- US patent 6473848 discloses a serial buffer turbo decoder.

7. Any inquiry concerning this communication from the examiner should be directed to Thomas M Ho whose telephone number is (571)272-3835. The examiner can normally be reached on M-F from 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory A. Morse can be reached on (571)272-3838.

The Examiner may also be reached through email through Thomas.Ho6@uspto.gov

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

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TMH

June 24th, 2005

David Y. Jung
Primary Examiner

6/25/05